

Matsumura does not produce compressed data at a single output on edges of a clock signal as is recited in claim 1. Matsumura does not describe the single bit ECMP as being produced relative to edges of a clock signal. Matsumura does say the following:

“a latch 4k which transfers and applies a signal of 1 bit [ECMP] from compression circuit 4j to a pad 8p in accordance with test clock signal ETCLK.” Matsumura, column 21, lines 22-26.

Matsumura does not mention edges of the test clock signal ETCLK. Also, the test clock signal ETCLK is not shown as being coupled to the compression circuit 4j and plays no role in compressing the 256 bits down into the single bit ECMP of Matsumura. The test clock signal ETCLK is apparently coupled to the latch 4k between the compression circuit 4j and the pad 8p and may play a role in transferring the single bit ECMP to the pad 8p. However, once compression takes place to generate the single bit ECMP, Matsumura does not say if it is changed or affected by edges of the test clock signal ETCLK.

The applicant respectfully submits that Matsumura does not show producing compressed data at a single output on edges of a clock signal as is recited in claim 1. The applicant respectfully submits that Matsumura does not show all of the elements recited in claim 1, and that claim 1 is in condition for allowance. Claim 2 is dependent on claim 1, and recites further limitations with respect to claim 1. For reasons analogous to those stated above, and the limitations in the claim, the applicant respectfully submits that Matsumura does not show all of the elements recited in claim 2, and that claim 2 is in condition for allowance.

Claims 4-6, 8-10, 12-28, 31-41, and 43-45 recite elements similar to those recited in claim 1. For reasons analogous to those stated above, and the limitations in the claims, the applicant respectfully submits that Matsumura does not show all of the elements recited in claims 4-6, 8-10, 12-28, 31-41, and 43-45, and that claims 4-6, 8-10, 12-28, 31-41, and 43-45 are in condition for allowance.

Claim 30 recites a memory device comprising a plurality of memory cells, means for compressing a plurality of data values read from selected ones of the memory cells into test data, and means for producing the test data on edges of a clock signal.

Claim 30 is a means-plus-function claim under 35 U.S.C. § 112, paragraph 6. The Office Action has not presented an explanation or a rationale as to why the showing of Matsumura is equivalent to the corresponding elements disclosed in the specification as is required by MPEP 2182 and 2183.

The applicant respectfully submits that Matsumura does not show an equivalent to the corresponding elements disclosed in the specification under 35 U.S.C. § 112, paragraph 6. Matsumura does not anticipate claim 30, and therefore claim 30 is in condition for allowance.

Rejection of Claims under §103

Claims 3, 7, 11, and 29 were rejected under 35 USC § 103(a) as being unpatentable over Matsumura in view of Schober (U.S. Patent No. 6,297,668). The applicant respectfully traverses.

Schober issued on 2 October 2001, which is after the 29 January 1999 filing date of the above-identified application. The applicant does not admit that Schober is prior art.

Schober mentions flip-flops, latches, and other circuits in column 9, lines 35-37, but the Office Action has not shown how Schober supplies the elements missing in Matsumura discussed above.

Claims 3, 7, 11, and 29 are dependent respectively on claims 1, 4, 8, and 26, and recite further limitations with respect to those claims. For reasons analogous to those stated above, and the limitations in the claims, the applicant respectfully submits that Matsumura and Schober do not show all of the elements recited in claims 3, 7, 11, and 29, and that claims 3, 7, 11, and 29 are in condition for allowance.

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney at (612) 373-6973 to facilitate prosecution of this application.

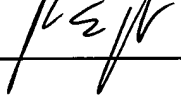
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Respectfully submitted,

MIRMAJID SEYYEDY ET AL.

By their Representatives,

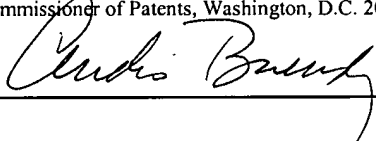
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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, Washington, D.C. 20231, on this 3rd day of January, 2003.

Candis B. Buending

Name



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